**Laboratory 3**

**External Memory Interface**

**Pre-Lab**

**Team Number 5**

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**LAB 3 – External Memory Interface**

For laboratory 3, we were asked to implement in the FPGA, two 8-bit memory-mapped input ports and two 8-bit memory-mapped output ports. The ports are to be mapped into the ARM memory space so that they are accessible in external memory region 0. We used minimal decoding as specified as to speed up the decoding logic at the cost of a larger usage of memory addresses.

Our decoding logic involves the P3\_0 pin, Read strobe, Write Strobe, and MS0. To account for the active low configuration of the read and write strobes, as well as MS0, not gates have been added. We have chosen to ignore the output of the decoder in which the read and write strobes are not simultaneously released or pressed. We are therefore using 4/8 states in which one or the other is selected.

We have also accounted for the fact that the decoded output pin of the 3:8 Decoder will be driven low, where the rest will be high… For this reason the inputs to the CLK of Output Port 0 and Output Port 1 have been negated.

Attached you will find the schematic demonstrating our usage of the FPGA to perform interfacing with I/O devices using the external memory interface.